



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

<b>In re U.S. Patent Application of</b>	)	
<b>YAMAMOTO et al.</b>	)	
<b>Application Number: 10/817,004</b>	)	<b>Art Unit 2826</b>
<b>Filed: April 5, 2004</b>	)	
<b>For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE</b>	)	<b>Examiner Ahmed N. Sefer</b>
<b>AND MANUFACTURING METHOD THEREOF</b>	)	
<b>ATTORNEY DOCKET NO. HITA.0536</b>	)	

**Honorable Assistant Commissioner  
for Patents  
Washington, D.C. 20231**

**RESPONSE TO RESTRICTION REQUIREMENT**

Sir:

This is in response to the Office Action mailed on May 6, 2005, the shortened period of response to which is set to expire on September 6, 2005, with the payment of the fee for a three-month extension of time. Applicants hereby elect the continuing prosecution of Species 3 as recited in claims 6 and 7, directed to the embodiment illustrated in Figures 10-11, without traverse.